

Faculty of Engineering

Computer and Systems Engineering Department

**CSE 311: Computer Organization (2)**

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Mips Processor Single Cycle Implementation

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1. **Description of the implementation :**

**Mips consists of :**

1. **PC:**

The program counter is a 32 bit D-flip flop register. It selects the address of the upcoming instruction. The PC is incremented after fetching the instruction and hold the memory address of the next instruction that will be executed.

**b) Instruction memory:**

It is a memory composed of a 32 bit width and in our implementation it has 40 entries depth. It holds the instructions that should be executed.

**c) Control Unit:**

It generates all control signals to all components of the processor .These control signals jump , branch , memread, memtoreg, aluop, memwrite , alu src ,regwrite and regdst.Its input is the opcode .

**d) Register File:**

It is an array of processor registers in a CPU.It has 32 registers each is of 32 bits. It holds the values of the registers on which operations are executed.

**e) ALU:**

It is the Arithmetic Logic Unit, a digital electronic circuit which performs bitwise arithmetic and logical operations.

It has two inputs .The first is Read Data 1 from the register file and the second is the output of the MUX that contains the Read Data 2 from register file and output from the sign extension unit.

**f) ALU control:**

Its inputs is the least six significant bits(function field ) and the other is the ALU op.It generates a control signal as an input to the ALU to select the operation to be executed.

**g) Data Memory:**

It has 256 registers each of width 32 bits.It holds the necessary data for instruction execution.

**h) Multiplexers:**

They are used to select one of its inputs to be forwarded to the next component depending on selector. Number of inputs is 2selectors .

**I) Sign extension:**

Its input is a 16 bit input and output is of 32 bits.It repeats the most significant bit of the input 16 times to be the most significant of the output.

**K) Full adder:**

It is a 32 bit full adder.

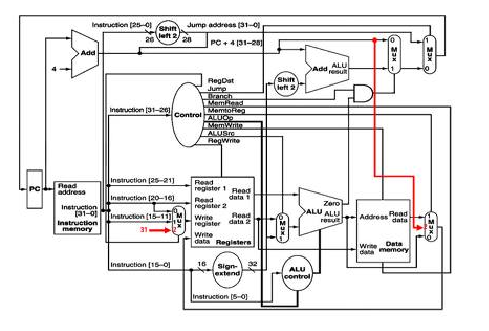
**L) Shift by two:**

Shifts the input by two.

**M) Adder(pc+4):**

Increments the program counter by four.

**2)Data path :**

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We added two changes:

1. The instruction [10:6] is a shift amount input for the ALU.
2. Jump register control signal is an output from ALU control unit to a third MUX whose output is an input to the program counter.

**3)How the work was split:**

1-Magdy Mohamed Abdel Moneim Hafez

* Instruction memory.
* Multiplexors.
* Program counter.

2-Mohamed Ismail Mohamed Hafez:

* ALU.
* ALU Control Unit.

3-Sherif Ahmed Hassan Kotb:

* Data memory.
* Shift by two unit.
* Full Adder.

4-Shady Hany El Sayed Mohamed:

* Control Unit.
* (PC+4) Adder.

5-Marco Emile Ramzy Andraws:

* Register File.
* Sign extension.
* The whole team contributed in the integration, testing and simulation of the MIPS.